

U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Serial No.	
				M-15297 US		10/797,972	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicant(s)			
(Use several sheets if necessary)				Yi Ding			
				Filing Date		Group	
				March 10, 2004		Unassigned	
U.S. Patent Documents							
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
AB	AA	5,402,371	28 Mar. 1995	Ono			
	AB	5,856,943	5 Jan. 1999	Jenq			
	AC	5,901,084	4 May 1999	Ohnakado			
	AD	6,057,575	2 May 2000	Jenq			
	AE	6,130,129	10 Oct. 2000	Chen			
	AF	6,134,144	17 Oct. 2000	Lin et al.			
	AG	6,171,909	9 Jan. 2001	Ding et al.			
	AH	6,200,856	13 Mar. 2001	Chen			
	AI	6,261,856	17 Jul. 2001	Chang et al.			
	AJ	6,266,278	24 Jul. 2001	Harari et al.			
	AK	6,326,661	4 Dec. 2001	Dormans et al.			
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	AM	6,365,457	2 Apr. 2002	Choi			
	AN	6,414,872	2 Jul. 2002	Bergemont et al.			
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	AR	6,486,023	26 Nov. 2002	Nagata			
	AS	6,518,618	11 Feb. 2003	Fazio et al.			
	AT	6,541,324	1 Apr. 2003	Wang			
AU	6,541,829	1 Apr. 2003	Nishinohara et al.				
AV	2002/0064071 A1	30 May 2002	Takahashi et al.				
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AX	2003/0218908 A1	27 Nov. 2003	Park et al.				
AY	2004/0004863 A1	8 Jan. 2004	Wang				
Examiner	Date Considered						
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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)			
<i>RA</i>	AZ	Wu, A.T.; Chan T.Y.; Ko, P.K.; and Hu, C. "A Novel High-Speed, 5-Volt Programming EPROM Structure With Source-Side Injection," 1986 IEEE, 584-587.	
	BA	Mizutani, Yoshihisa; and Makita, Koji "A New EPROM Cell With A Sidewall Floating Gate Fro High-Density and High Performance Device," 1985 IEEE, 635-638.	
	BB	Ma, Y.; Pang, C.S.; Pathak, J.; Tsao, S.C.; Chang, C.F.; Yamauchi, Y.; Yoshimi, M. "A Novel High Density Contactless Flash Memory Array Using Split-Gate Source-Side-Injection Cell for 5V-Only Applications," 1994 Symposium on VLSI Technology Digest of Technical Papers, pages 49-50.	
	BC	Mih, Rebecca et al. "0.18um Modular Triple Self-Aligned Embedded Split-Gate Flash Memory," 2000 Symposium on VLSI Technology Digest of Technical Papers, pages 120-121.	
	BD	Ma, Yale et al., "A Dual-Bit Split-Gate EEPROM (DSG) Cell in Contactless Array for Single Vcc High Density Flash Memories," 1994 IEEE, 3.5.1-3.5.4.	
	BE	Spinelli, Alessandro S., "Quantum-Mechanical 2D Simulation of Surface-and Buried-Channel p-MOS," 2000 International Conference on Simulation of Semiconductor Processes and Devices: SISPAD 2000, Seattle, WA September 6-8, 2000	
	BF	Kim, K.S. et al. "A Novel Dual String NOR (DuSnor) Memory Cell Technolgy Scalabe to the 256 Mbit and 1 Gbit Flash Memories," 1995 IEEE 11.1.1-11.1.4	
	BG	Bergemont, A. et al. "NOR Virtual Ground (NVG)- A New Scaling Concept for Very High Density FLAS EEPROM and its Implementation in a 0.5 um Process," 1993 IEEE 2.2.1-2.2.4	
	BH	Van Duuren, Michiel et al., "Compact poly-CMP Embedded Flash Memory Cells For One or Two Bit Storage," Philips Research Leuven, Kapeldreef 75, B3001 Leuven, Belgium, pages 73-74.	
	BI	United States Patent Application No. 10/440,466, entitled "Fabrication Of Conductive Gates For Nonvolatile Memories From Layers With Protruding Portions," Filed on May 16, 2003; Attorney Docket No.: M-12979 US.	
	BJ	United States Patent Application No. 10/440,005, entitled "Fabrication of Dielectric On A Gate Surface To Insulate The Gate From Another Element Of An Integrated Circuit," Filed on May 16, 2003; Attorney Docket No.: M-15203 US.	
	BK	United States Patent Application No. 10/440,508, entitled "Fabrication Of Gate Dielectric In Nonvolatile Memories Having Select, Floating And Control Gates," Filed on May 16, 2003; Attorney Docket No.: M-15204 US.	
	BL	United States Patent Application No. 10/440,500, entitled "Integrated Circuits With Openings that Allow Electrical Contact To Conductive Features Having Self-Aligned Edges," Filed on May 16, 2003; Attorney Docket No.: M-15205 US.	
<i>RA</i>	BM	United States Patent Application No. 10/393,212, entitled "Nonvolatile Memories And Methods Of Fabrication," Filed on March 19, 2003; Attorney Docket No.: M-12902 US.	
Examiner <i>Robert AA</i>	Date Considered <i>06/26/05</i>		
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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
NA	BN	United States Patent Application No. 10/411,813, entitled "Nonvolatile Memories With A Floating Gate Having An Upward Protrusion," Filed on April 10, 2003; Attorney Docket No.: M-12903 US.						
	BO	United States Patent Application No. 10/393,202, entitled "Fabrication of Integrated Circuit Elements In Structures With Protruding Features," Filed on March 19, 2003; Attorney Docket No.: M-15151 US.						
	BP	United States Patent Application No. 10/631,941, entitled "Nonvolatile Memory Cell With Multiple Floating Gates Formed After The Select Gate," Filed on July 30, 2003; Attorney Docket No.: M-15171 US.						
	BQ	United States Patent Application No. 10/632,155, entitled "Nonvolatile Memory Cells With Buried Channel Transistors," Filed on July 30, 2003; Attorney Docket No.: M-15222 US.						
	BR	United States Patent Application No. 10/632,007, entitled "Arrays Of Nonvolatile Memory Cells Wherin Each Cell Has Two Conductive Floating Gates," Filed on July 30, 2003; Attorney Docket No.: M-15223 US.						
	BS	United States Patent Application No. 10/631,452, entitled "Fabrication Of Dielectric For A Nonvolatile Memory Cell Having Multiple Floating Gates," Filed on July 30, 2003; Attorney Docket No.: M-15229 US.						
	BT	United States Patent Application No. 10/632,154, entitled "Fabrication Of Gate Dielectric In Nonvolatile Memories In Which A Memory Cell Has Mutple Floating Gates," Filed on July 30, 2003; Attorney Docket No.: M-15230 US.						
	BU	United States Patent Application No. 10/632,186, entitled "Nonvolatile Memory Cell With Multiple Floating Gates Formed After The Select Gate And Having Upward Protrusions," Filed on July 30, 2003; Attorney Docket No.: M-15241 US.						
	BV	United States Patent Application No. 10/631,552, entitled "Nonvolatile Memories And Methods Of Fabrication," Filed on July 30, 2003; Attorney Docket No.: M-12902-1P US.						
	BW	Shirota, Riichiro "A Review of 256Mbit NAND Flash Memories and NAND Flash Future Trend," February 2000, Nonvolatile Memory Workshop in Monterey, California, pages 22-31.						
NA	BX	United States Patent Application No. 10/798,475, entitled "Fabrication Of Conducted Lines Interconnecting Conductive Gates In Nonvolatile Memories And Non-Volatile Memory Structures," Filed on March 10, 2004; Attorney Docket No.: M-15296 US.						
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
NA	BY	EP 0 938 098 A2	25 Aug. 1999	Europe				
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